

Features

- Low On-Resistance (33ohm typ) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors in Sample-and-Holds. Charge Injection, 2pC typ
- Single-Supply Operation (+2.5V to +16V)
- Improved Second Sources for MAX4501/MAX4502
- On-Resistance Matching Between Channels, <2ohm
- On-Resistance Flatness, <6ohm max
- Low Off-Channel Leakage, <5nA @ +85°C
- TTL/CMOS Logic Compatible
- Fast Switching Speed, $t_{ON} < 150\text{ns}$
- Guaranteed Break-Before-Make action (PS303 only) eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Dynamic Range
- Low Power Consumption, <5 μW
- MSOP Package minimizes board area

Applications

- Audio, Video Switching and Routing
- Portable Instruments
- Data Acquisition Systems
- Sample-and-Holds
- Telecommunication Systems
- Battery-Powered Systems

Description

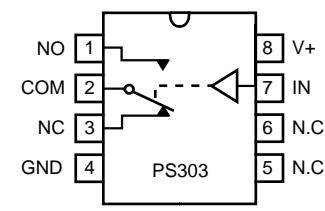
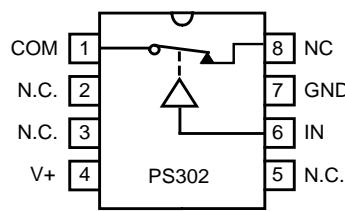
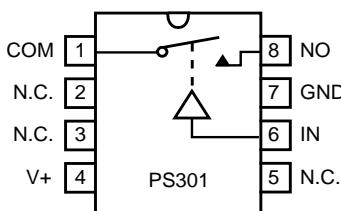
The PS301/PS302/PS303 are improved high precision, medium voltage analog switches designed to operate with single power supplies. The PS301 is a single-pole single-throw (SPST), normally open (NO) switch. The PS302 has the same pinout as the PS301 but is a normally closed (NC) switch. The PS303 has one normally open (NO) and one normally closed (NC) switch per package. Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rail.

With a +5V power supply, the PS301/PS302/PS303 guarantee <60ohm ON-resistance. ON-resistance matching between channels is within 2ohm. ON-resistance flatness is less than 6ohm over the specified range. All three devices guarantee low leakage currents (<100pA @ 25°C, <10nA @ +85°C) and fast switching speeds ($t_{ON} < 150\text{ns}$). Break-before-make switching action protects against momentary crosstalk (PS303).

For single-supply operation below 5V, the PI5A317/318/319 are also recommended.

Functional Diagrams, Pin Configurations, and Truth Tables

Top Views



Switches shown for logic “0” input

PS301	
Logic	Switch
0	OFF
1	ON

PS302	
Logic	Switch
0	ON
1	OFF

Logic	NC	NO
0	ON	OFF
1	OFF	ON

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Absolute Maximum Ratings

Voltages Referenced to GND	
V ⁺	-0.3V to +17V
V _{IN} , V _{COM} , V _{NC} , V _{NO} (Note 1)	-2V to (V ⁺) +2V or 30mA, whichever occurs first
Current (any terminal)	
Peak Current, COM, NO, NC (pulsed at 1ms, 10% duty cycle)	30mA 100mA
ESD per Method 3015.7	>2000V

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +5V Supply (V⁺ = 5V +10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}	V ⁺ = 4.5V, V _{NO} or V _{NC} = +3.5V, I _{COM} = 1mA	25		33	60	V
On Resistance	R _{ON}		Full			75	
On-Resistance Match Between Channels ⁽⁴⁾							
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}	V _{NO} or V _{NC} = +3V, I _{COM} = 1mA, V ⁺ = 5V	25		0.8	2	ohm
			Full			4	
NO or NC Off Leakage Current ⁽⁶⁾	I _{NO(OFF)} or I _{NC(OFF)}	V ⁺ = 5.5V, V _{COM} = 1V, V _{NO} or V _{NC} = 4.5V	25		2	6	nA
			Full			8	
COM Off Leakage Current ⁽⁶⁾	I _{COM(OFF)}	V ⁺ = 5.5V, V _{COM} = 4.5V, V _{NO} or V _{NC} = 1V	25	-0.1	-0.01	0.1	nA
			Full	-5		5	
COM On Leakage Current ⁽⁶⁾	I _{COM(ON)}	V ⁺ = 5.5V, V _{COM} = 5V, V _{NO} or V _{NC} = 5V	25	-0.2	-0.04	0.2	V
			Full	-10		10	
Logic Input							
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V	Full	-0.5	0.005	0.5	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-0.5	0.005	0.5	
Logic High Input Voltage	V _{INH}			2.4			V
Logic Low Input Voltage	V _{INL}					0.8	

Electrical Specifications - Single +5V Supply (continued)
 $(V_+ = 5V \pm 10\%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)$

Parameter	Symbol	Conditions	Temp. (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Dynamic							
Turn-On Time	t_{ON}	V_{NO} or $V_{NC} = 3V$, Figure 2	25		85	150	ns
			Full			240	
Turn-Off Time	t_{OFF}		25		25	100	
			Full			150	
Break-Before-Make TimeDelay ⁽³⁾	t_D	PS303 only, $R_L = 300\text{ohm}$, $C_L = 35\text{pF}$, Fig. 3	25	2	5		pC
Charge Injection ⁽³⁾	Q	$C_L = 1\text{nF}$, $V_{GEN} = 0V$, $R_{GEN} = 0\text{ohm}$, Fig. 4			1	5	
Off Isolation ⁽⁷⁾	OIRR	$R_L = 50\text{ohm}$, $C_L = 5\text{pF}$, $f = 1\text{MHz}$, Fig. 5			-72		dB
Crosstalk	X_{TALK}	$R_L = 50\text{ohm}$, $C_L = 5\text{pF}$, $f = 1\text{MHz}$, Fig. 6			-85		
NC or NO Off Capacitance	$C_{(OFF)}$	$f = 1\text{MHz}$, Figure 7	25		9		pF
COM Off Capacitance	$C_{COM(OFF)}$				9		
COM On Capacitance	$C_{COM(ON)}$				22		
Supply							
Power-Supply Range	V_+		Full	2.7		16	V
Positive Supply Current	I_+	$V_+ = 5.5V$, $V_{IN} = 0V$ or V_+ , all channels on or off		-1		1	μA

Notes:

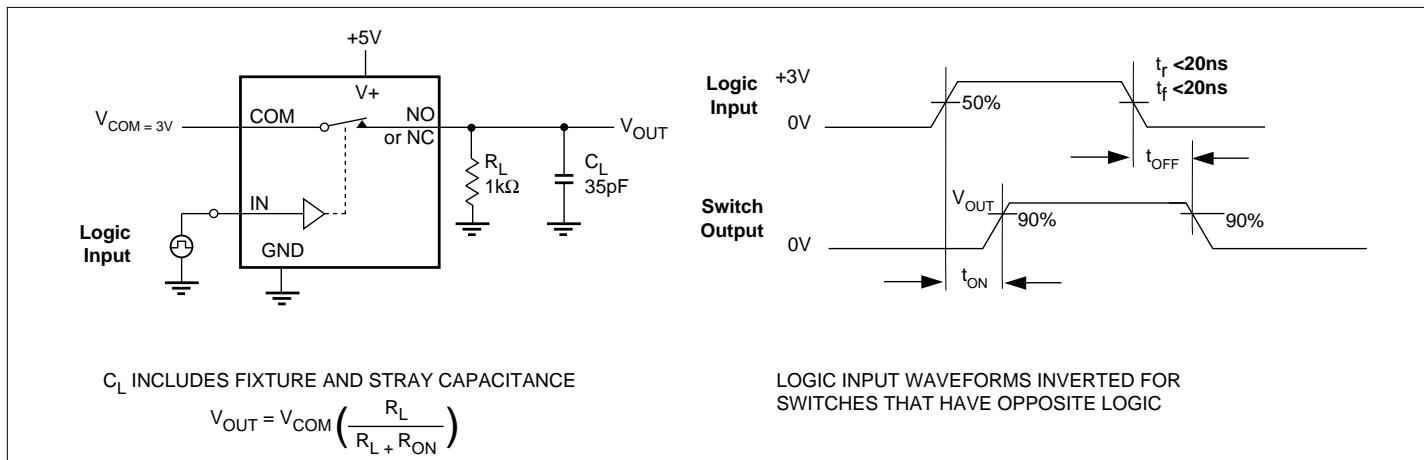
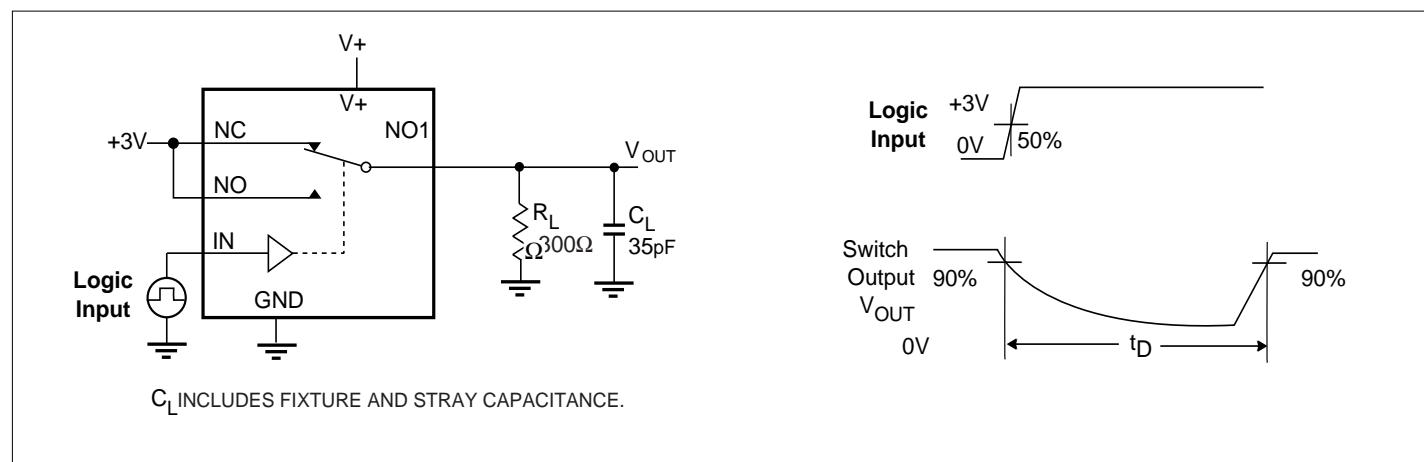
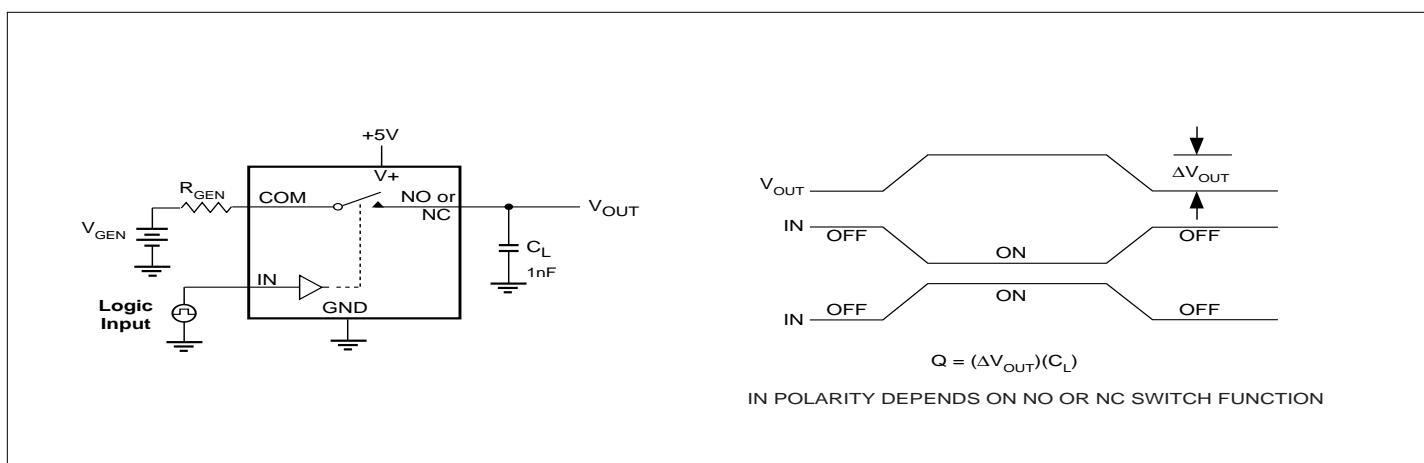
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON \text{ max.}} - R_{ON \text{ min.}}$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $+25^\circ\text{C}$.
7. Off Isolation = $20\log_{10} [V_{COM} / (V_{NC} \text{ or } V_{NO})]$. See Figure 5.

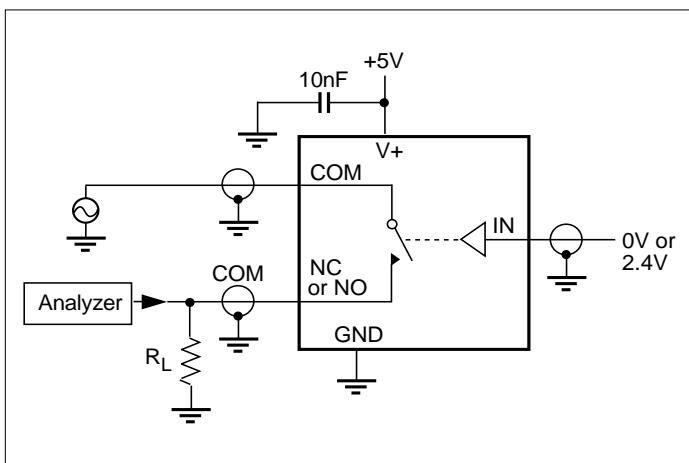
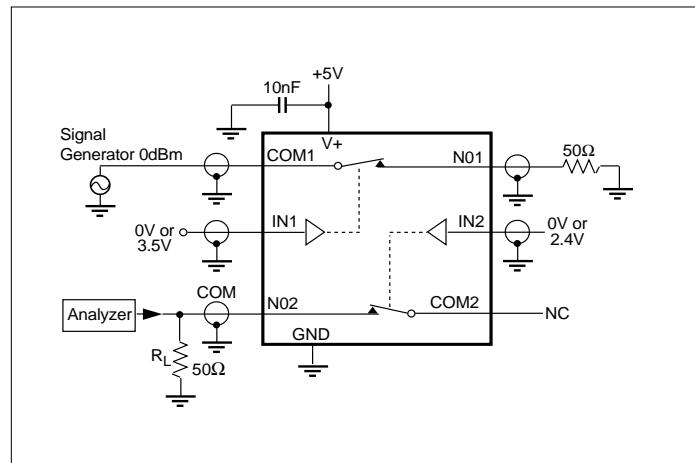
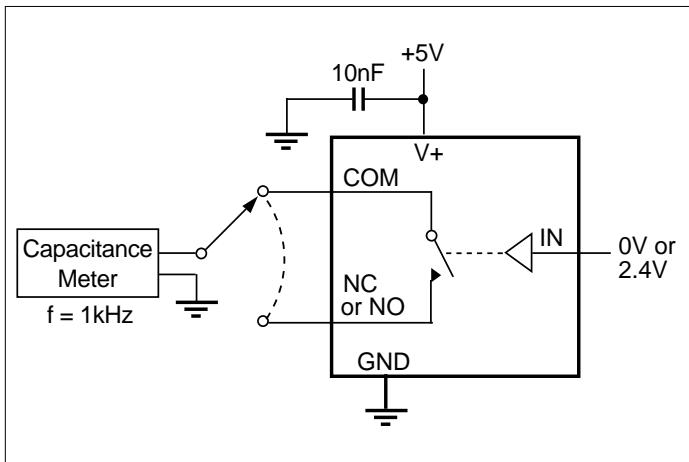
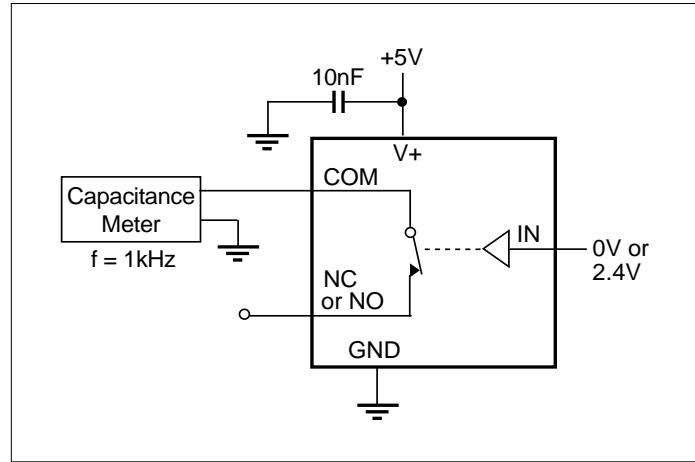
Electrical Specifications - Single +12V Supply
 $(V+ = 12V \pm 10\%, GND = 0V, V_{INH} = 5V, V_{INL} = 0V)$

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units	
Analog Switch								
Analog Signal Range ⁽³⁾	V_{ANALOG}			0		$V+$	V	
On-Resistance	R_{ON}	$V+ = 12V, I_{COM} = 1mA, V_{NO} \text{ or } V_{NC} = 6V$	25		14	35	ohm	
			Full			45		
Dynamic								
Turn-On Time ⁽³⁾	t_{ON}	$V_{NO} \text{ or } V_{NC} = 6V, \text{ Figure 2}$	25		85	150	ns	
			Full			240		
Turn-Off Time ⁽³⁾	t_{OFF}		25		25	100		
			Full			150		
Break-Before-Make Time Delay ⁽³⁾	t_D	PS303 only	25	2	5			
Charge Injection ⁽³⁾	Q	$C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0\text{ohm}, \text{ Figure 4}$	25				pC	
Supply								
Positive Supply Current	$I+$	$V+ = 13.2V, V_{IN} = 0V \text{ or } V+, \text{ all channels on or off}$	Full	-1	0.01	1	μA	

Electrical Specifications - Single +3.3V Supply
 $(V+ = 3.3V \pm 10\%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)$

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units	
Analog Switch								
Analog Signal Range ⁽³⁾	V_{ANALOG}			0		$V+$	V	
On-Resistance	R_{ON}	$V+ = 3V, I_{COM} = 1mA, V_{NO} \text{ or } V_{NC} = 1.5V$	25		83	175	ohm	
			Full			275		
Dynamic								
Turn-On Time ⁽³⁾	t_{ON}	$V_{NO} \text{ or } V_{NC} = 1.5V, \text{ Figure 2}$	25		160	400	ns	
			Full			500		
Turn-Off Time ⁽³⁾	t_{OFF}		25		40	125		
			Full			175		
Break-Before-Make Time Delay ⁽³⁾	t_D	PS303 only	25	2	5			
Charge Injection ⁽³⁾	Q	$C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0\text{ohm}, \text{ Figure 4}$	25		1	5	pC	
Supply								
Positive Supply Current	$I+$	$V+ = 3.6V, V_{IN} = 0V \text{ or } V+, \text{ all channels on or off}$	Full	-1	0.01	1	μA	

Test Circuits/Timing Diagrams

Figure 2. Switching Time

Figure 3. Break-Before-Make Interval (PS303 only)

Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

Figure 5. Off Isolation

Figure 6. Crosstalk

Figure 7. Channel-Off Capacitance

Figure 8. Channel-On Capacitance

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

Logic Levels

When powered from +5V the PS301/PS302/PS303 can be operated with either TTL- or CMOS-Logic levels. If V+ is different than +5V, the logic threshold level will vary.

Power consumption is minimal when the logic control voltages reach V+ or GND.

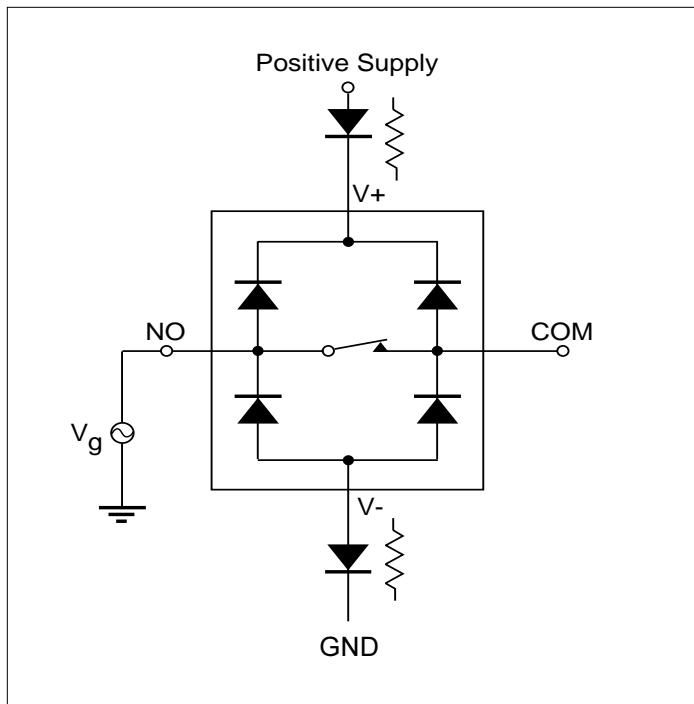


Figure 1. Overvoltage protection is accomplished by using two external blocking diodes or two current limiting resistors.

Ordering Information

Part	Temp. Range	Package
PS301CPA	0°C to +70°C	8 Plastic DIP
PS301CSA	0°C to +70°C	8 Narrow SO
PS301CUA	0°C to +70°C	8 MSOP
PS301EPA	-40°C to +85°C	8 Plastic DIP
PS301ESA	-40°C to +85°C	8 Narrow SO
PS302CPA	0°C to +70°C	8 Plastic DIP
PS302CSA	0°C to +70°C	8 Narrow SO
PS302CUA	0°C to +70°C	8 MSOP

Part	Temp. Range	Package
PS302EPA	-40°C to +85°C	8 Plastic DIP
PS302ESA	-40°C to +85°C	8 Narrow SO
PS303CPA	0°C to +70°C	8 Plastic DIP
PS303CSA	0°C to +70°C	8 Narrow SO
PS303CUA	0°C to +70°C	8 MSOP
PS303EPA	-40°C to +85°C	8 Plastic DIP
PS303ESA	-40°C to +85°C	8 Narrow SO